DATA SHEET

BSP120
N-channel enhancement mode vertical D-MOS transistor

Product specification
File under Discrete Semiconductors, SC13b

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Philips
Semiconductors

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N-channel enhancement mode vertical D-MOS transistor

BSP120

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Drain-current (DC)	I_D	max.	250	mA
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	7 12	Ω Ω
Gate threshold voltage	$V_{GS(th)}$	max.	2.8	V

PINNING - SOT223

1 = gate
2 = drain
3 = source
4 = drain

Marking code

BSP120

PIN CONFIGURATION

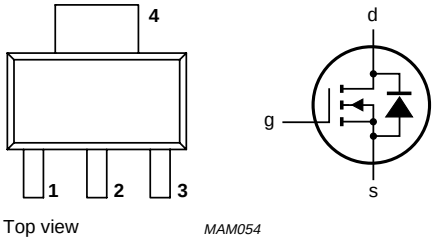


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSP120

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200	V
Drain-source leakage current				
V_{DS} =160 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current				
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Drain-source ON-resistance (see Fig.4)				
I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	7 12	Ω Ω
Gate threshold voltage				
I_D = 1 mA; V_{GS} = V_{DS}	$V_{GS(th)}$	min. max.	0.8 2.8	V V
Transfer admittance				
I_D = 250 mA; V_{DS} = 15 V	$\lvert Y_{fs} \rvert$	min. typ.	125 250	mS mS
Input capacitance at f = 1 MHz;				
V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 65	pF pF
Output capacitance at f = 1 MHz;				
V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 30	pF pF

Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	3 ns 6 ns
	t_{off}	typ. max.	15 ns 20 ns

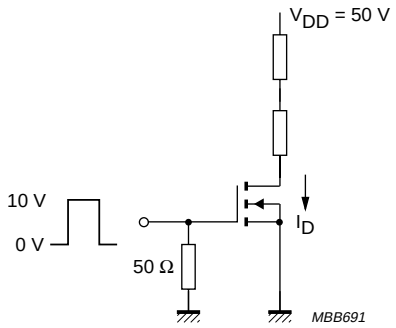


Fig.2 Switching time test circuit.

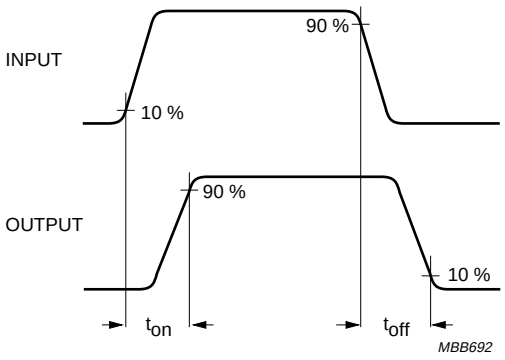


Fig.3 Input and output waveforms.

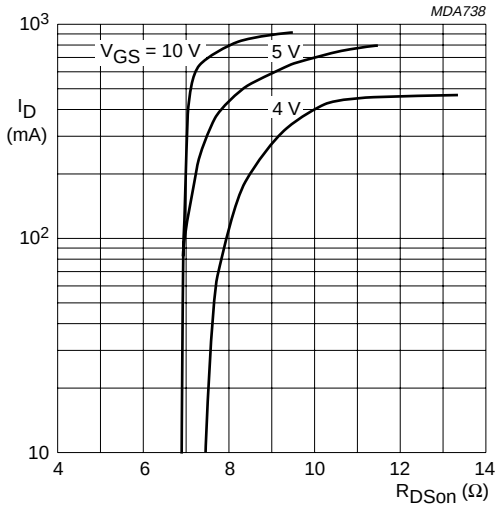


Fig.4 T_j = 25 °C; typical values.

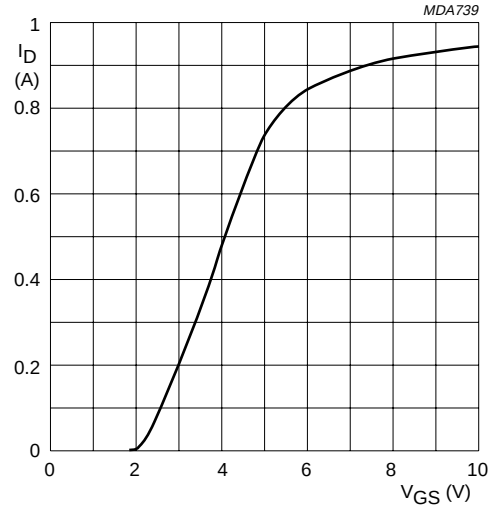


Fig.5 T_j = 25 °C; V_{DS} = 10 V; typical values.

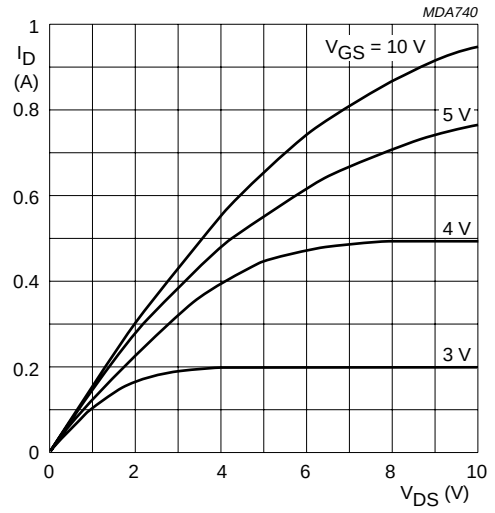


Fig.6 T_j = 25 °C; typical values.

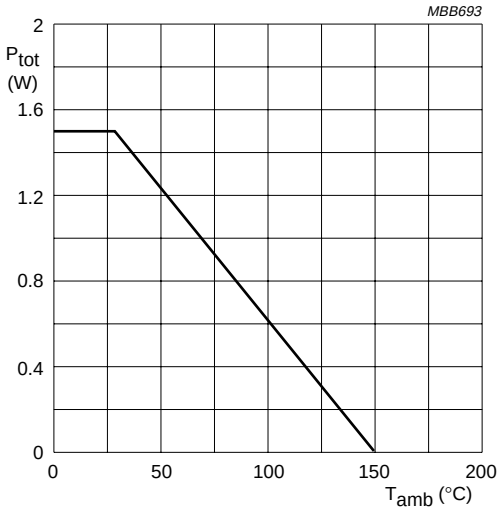


Fig.7 Power derating curve.

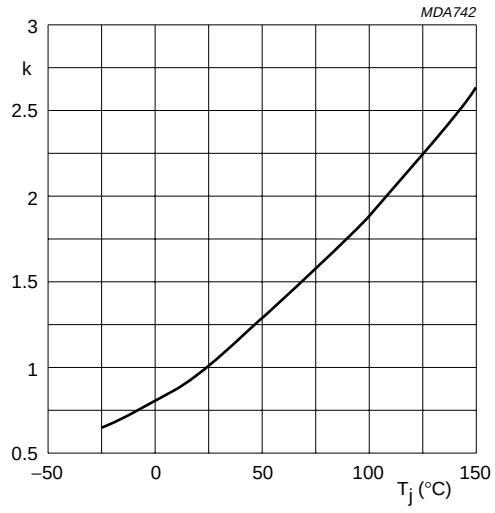


Fig.8

$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C};$$

at 250 mA/10 V; typical values.

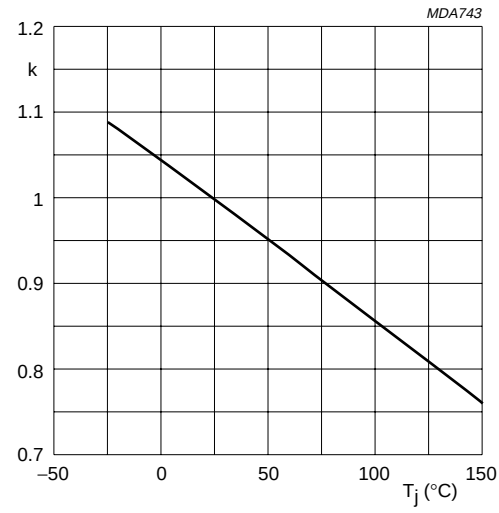


Fig.9

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

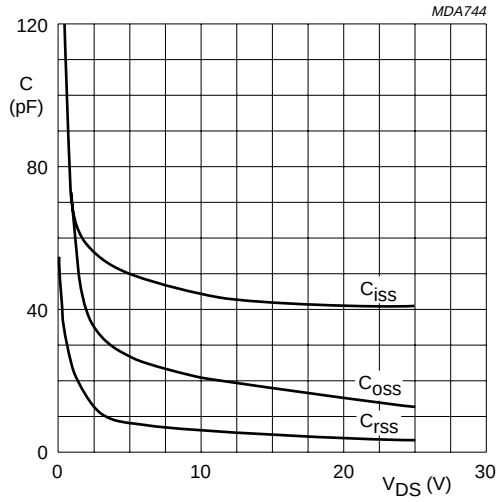
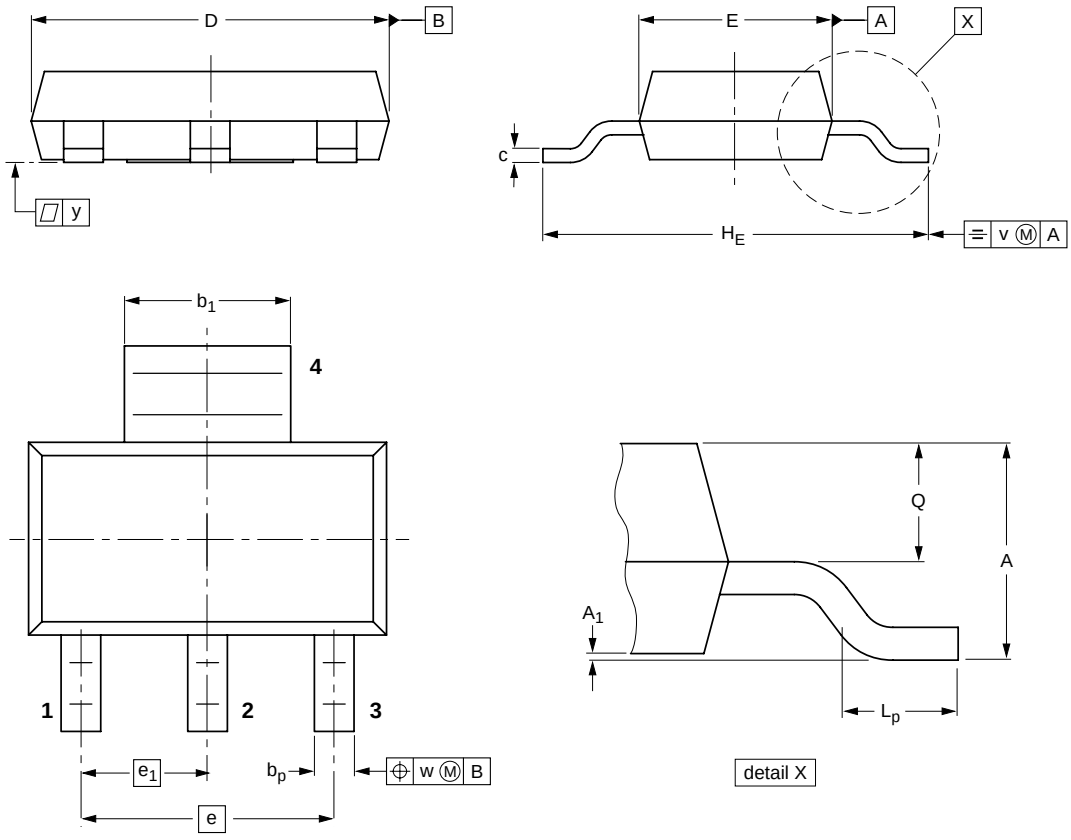


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						~~96-11-11~~ 97-02-28

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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